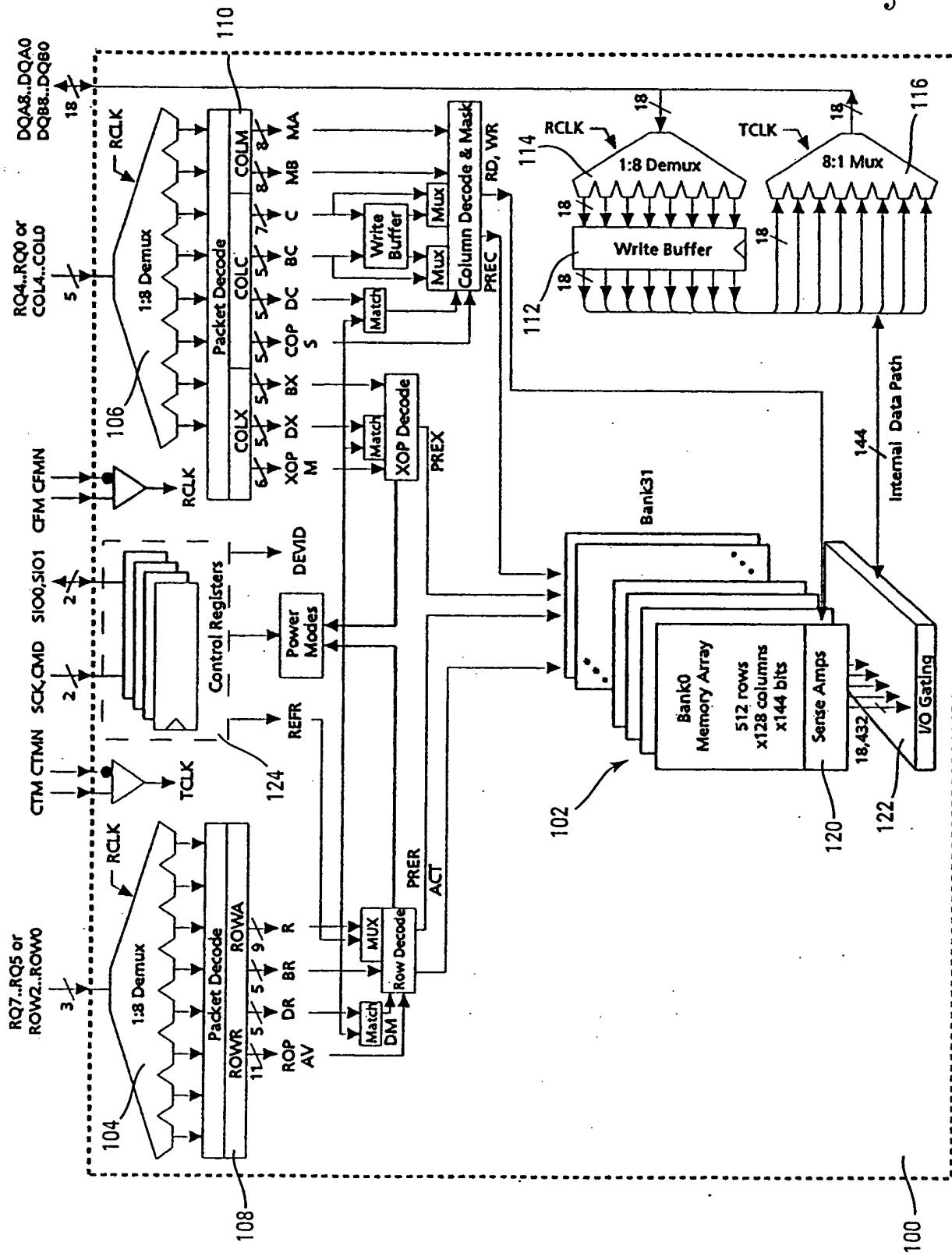
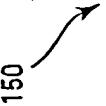


Fig. 1



150



(TOP VIEW)

10	V _{DD}	GND		V _{DD}	GND	V _{DD}			V _{DD}	V _{DD}		GND	V _{DD}	
9														
8	V _{DD}	CMD	GND	GND _a	GND _a	V _{DD}	V _{DD}	GND	V _{DD}	V _{DD}	GND	GND	V _{DD}	
7	DQA8	DQA7	DQA5	DQA3	DQA1	CTMN	CTMN	RQ7	RQ5	RQ3	RQ1	DQB1	DQB3	DQB5
6														DQB7
5														DQB8
4	GND	DQA6	DQA4	DQA2	DQA0	CFM	CFMN	RQ6	RQ4	RQ2	RQ0	DQB0	DQB2	DQB4
3	GND	SCK	VCMOS	GND	V _{DD}	GND	V _{DDA}	V _{REF}	GND	GND	GND	DQB6	DQB6	GND
2														
1	V _{DD}		GND		GND	V _{DD}	GND					GND	GND	GND
	A	B	C	D	E	F	G	H	I	J	K	L	M	N
												R	S	

Fig. 2